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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/981,872	10/18/2001	Patrick Joseph Bohrer	AUS920010150US1	7091

7590 09/22/2004

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EXAMINER	
SURYAWANSHI, SURESH	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/981,872	BOHRER ET AL.	
	Examiner	Art Unit	
	Suresh K Suryawanshi	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 are presented for examination.

Specification

2. The abstract of the disclosure is objected to because it contains more than 150 words. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Howard et al (US Patent no 5,711,691 B1).

5. As per claims 1, 11 and 21, Howard et al disclose an energy management in a computer system having a plurality of computation nodes [col. 2, lines 7-13; computer system having a plurality of processors]. Howard et al teach awakening one or more of the processors from an inactive mode to an active mode when the processing workload is heavy and vice versa [Fig. 1A; col. 2, lines 15-30; col. 4, lines 27-58]. Howard et al clearly disclose of having an operational node [col. 5, lines 12-22; active processor(s)]; a standby node [col. 6, lines 23-27; col. 8, lines 45-49; nap state in which the processor clock is running and coherent cache storage for the processor is maintained]; and a hibernating node [col. 5, lines 12-22; placing one or more of the

processors in sleep mode where in the sleep mode, a processor will be shutdown; col. 15, lines 22-24, 34-38, 42-50].

Howard et al do not expressly disclose about having all the three modes of operations being utilized at the same time. Howard et al disclose utilizing two different modes of operations at the same time [col. 2, lines 15-30; col. 8, lines 41-64; active mode and sleep (inactive) mode; active mode and doze mode; nap mode and sleep mode]. However, a routineer in the art would be able to modify the invention to utilize the other modes of operations as detailed by Howard et al [col. 16, lines 47-48; each of the processors can operate in a run mode, a doze mode, a nap mode and a sleep mode] and have more than three nodes operating in three different modes of operations at the same time. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have three states of operating modes for a plurality of processors in a computer system being utilized same time. Moreover, having only two states of operation (active and inactive) will definitely provide a better power conservation since during a light workload most of the processing nodes will be in sleep mode (powered down). But, this also creates a problem of bringing online an inactive node quickly as the inactive node has to be turned on first whereas a processor in a nap (standby) mode can be brought online immediately to handle the workload because the processor is already on but at a low power mode. It will be advantageous to have a processor in a standby mode with active processor(s) in case there is an increase in workload while keeping remaining processors in hibernating mode. Thus, one can minimize the energy consumption without sacrificing in performance for the overall system.

6. As per claims 2, 12 and 22, Howard et al disclose about a lower and an upper computational workload limit [col. 4, lines 27-58; heavy or light workload].

7. As per claims 3, 13 and 23, Howard et al disclose about moving a computation node under operational node to hibernating node set when the workload is light [col. 4, lines 27-58].

8. As per claims 4, 14 and 24, Howard et al disclose about adding one or more additional processors when the workload is greater than the upper limit such that the combined workload of operational node set is less than the upper limit [col. 27-58].

9. As per claims 5, 15 and 25, Howard et al clearly disclose of having an operational node [col. 5, lines 12-22; active processor(s)]; a standby node [col. 6, lines 23-27; col. 8, lines 45-49; nap state in which the processor clock is running and coherent cache storage for the processor is maintained]; and a hibernating node [col. 5, lines 12-22; placing one or more of the processors in sleep mode where in the sleep mode, a processor will be shutdown; col. 15, lines 22-24, 34-38, 42-50]. Howard et al do not expressly disclose about having all the three modes of operations being utilized at the same time. Howard et al disclose utilizing two different modes of operations at the same time [col. 2, lines 15-30; col. 8, lines 41-64; active mode and sleep (inactive) mode; active mode and doze mode; nap mode and sleep mode]. However, a routineer in the art would be able to modify the invention to utilize the other modes of operations as detailed by Howard et al [col. 16, lines 47-48; each of the processors can operate in a run mode,

a doze mode, a nap mode and a sleep mode] and have more than three nodes operating in three different modes of operations at the same time. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have three states of operating modes for a plurality of processors in a computer system being utilized same time. Moreover, having only two states of operation (active and inactive) will definitely provide a better power conservation since during a light workload most of the processing nodes will be in sleep mode (powered down). But, this also creates a problem of bringing online an inactive node quickly as the inactive node has to be turned on first whereas a processor in a nap (standby) mode can be brought online immediately to handle the workload because the processor is already on but at a low power mode. It will be advantageous to have a processor in a standby mode with active processor(s) in case there is an increase in workload while keeping remaining processors in hibernating mode. Thus, one can minimize the energy consumption without sacrificing in performance for the overall system.

10. As per claims 6, 16 and 26, Howard et al disclose that computer system is a massively parallel processors system [Fig. 1C; processors A to D].

11. As per claims 7, 17 and 27, Howard et at disclose that computation node comprises a single processor [Fig. 1C; processor A is a computation node].

12. As per claims 8, 18 and 28, Howard et al disclose that computer system is a symmetrical multiprocessor system [Fig. 1C; processors A to D].

13. As per claims 9, 19 and 29, Howard et al disclose that computation node comprises multiple processors coupled to a shared memory unit [Fig. 1C; as whole computation node 100 comprises multiple processors A to D coupled to a shared memory unit 114].

14. As per claims 10, 20 and 30, Howard et al disclose that last active processor can be placed on different low power modes to minimize energy consumption [col. 5, lines 23-45].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K Suryawanshi whose telephone number is 703-305-3990 (starting 10/18/04, please use 571-272-3668). The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 703-305-9717 (starting 10/18/04, please use 571-272-3667). The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sks

September 16, 2004

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100